

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

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|------------------|--|-----------------|---------------------------|
| Applicant: | Torsten Partsch | Examiner: | Michael B. McFadden |
| Serial No.: | 10/706,438 | Group Art Unit: | 2188 |
| Filed: | November 12, 2003 | Docket: | Q331.102.101/2003P52601US |
| Due Date: | April 12, 2008 | | |
| Title: | RANDOM ACCESS MEMORY WITH OPTIONAL COLUMN ADDRESS STROBE LATENCY OF ONE | | |

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on February 12, 2008, appealing the final rejection of claims 1-38 of the above-identified application as set forth in the Final Office Action mailed December 12, 2007.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 50-0471 in the amount of \$10.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. § 41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 50-0471.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-38.

Appeal Brief to the Board of Patent Appeals and Interferences

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REAL PARTY IN INTEREST

The intellectual property embodied in the pending application is assigned to Infineon Technologies AG.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed December 12, 2007, claims 1-38 were finally rejected. Claims 1-38 are pending in the application. Claims 1-38 are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed December 12, 2007.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The subject matter of the claims involved in the Appeal is related to a random access memory.

One aspect of the present invention, as claimed in independent claim 1, provides a random access memory (10). The random access memory (10) includes an array of memory cells (32) and a memory (116a-116d) configured to receive data from the array of memory cells (32). The random access memory (10) includes a bypass circuit (114) configured to receive the data from the array of memory cells (32) and to bypass the memory (116a-116d). The random access memory (10) includes a circuit (118, 112, 113, 150, 156) configured to select between receiving the data from the memory (116a-116d) to provide first output signals and receiving the data from the bypass circuit (114) to provide second output signals based on a column address strobe latency select signal. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

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Another aspect of the present invention, as claimed in dependent claim 8, provides a random access memory (10). The random access memory (10) includes an array of memory cells (32) and a memory (116a-116d) configured to receive data from the array of memory cells (32). The random access memory (10) includes a bypass circuit (114) configured to receive the data from the array of memory cells (32) and to bypass the memory (116a-116d). The random access memory (10) includes a circuit (118, 112, 113, 150, 156) configured to select between receiving the data from the memory (116a-116d) to provide first output signals and receiving the data from the bypass circuit (114) to provide second output signals based on a column address strobe latency select signal. The circuit (118, 112, 113, 150, 156) includes a first circuit (118) configured to receive first rise and fall signals to serialize the data from the memory (116a-116d). The circuit (118, 112, 113, 150, 156) includes a second circuit (150) configured to receive second rise and fall signals to serialize the data from the bypass circuit (114). The circuit (118, 112, 113, 150, 156) includes a multiplexer (156) configured to select between serialized data from the first circuit (118) and serialized data from the second circuit (150) based on the column address strobe latency select signal. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Yet another aspect of the present invention, as claimed in independent claim 17, provides a random access memory (10). Random access memory (10) includes a first in/first out memory (116a-116d) and a bypass circuit (114) that bypasses the first in/first out memory (116a-116d). The random access memory (10) includes a control circuit (112, 113) configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory (116a-116d) to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit (114) to provide a column address strobe latency of one. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Yet another aspect of the present invention, as claimed in independent claim 25, provides a random access memory (10). The random access memory (10) includes a memory circuit (116a-116d) and a bypass circuit (114) configured to bypass the memory circuit (116a-116d). The random access memory (10) includes a first rise/fall circuit (118) configured to receive data from the memory circuit (116a-116d) to provide a first output

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signal and a second rise/fall circuit (150) configured to receive data from the bypass circuit (114) to provide a second output signal. The random access memory (10) includes a multiplexer (156) configured to select between the first output signal and the second output signal based on a column address strobe latency select signal. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Yet another aspect of the present invention, as claimed in independent claim 31, provides a random access memory (10). The random access memory (10) includes means (116a-116d) for storing data read from an array of memory cells (32) and means (114) for receiving the data read from the array of memory cells (32) to bypass the means (116a-116d) for storing data. The random access memory (10) includes means (118, 112, 113, 150, 156) for retrieving the data from the means (116a-116d) for storing the data if column address strobe latency is greater than one and means (118, 112, 113, 150, 156) for retrieving the data from the means (114) for receiving the data if the column address strobe latency is one. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

Yet another aspect of the present invention, as claimed in independent claim 34, provides a method for reading data from a random access memory (10) in a column address strobe latency of one. The method includes initiating a read command on a first edge of a clock cycle, receiving data read from the array of memory cells (10) in a bypass circuit (114) during the clock cycle, and retrieving the data from the bypass circuit (114) during the clock cycle. *See Specification*, at page 3, line 1 through line 32; page 6, line 18 through page 9, line 19; and Figures 1, 3, and 4.

GROUND'S OF REJECTION TO BE REVIEWED ON APPEAL

- I. Whether claims 1-3 and 31 are patentable under 35 U.S.C. § 102(b) over Usami, U.S. Patent No. 6,205,516 ("Usami"); whether claims 4-7, 9-16, 32, and 33 are patentable under 35 U.S.C. § 103(a) over Usami; and whether claims 1-7, 9-16, 32, and 33 are patentable under 35 U.S.C. § 103(a) over Usami in view of Sakamoto et al., "A Digitally Programmable Delay Chip with Picosecond Resolution" ("Sakamoto").

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- II. Whether claim 8 is patentable under 35 U.S.C. § 103(a) over Usami and whether claim 8 is patentable under 35 U.S.C. § 103(a) over Usami in view of Sakamoto.
- III. Whether claims 17 and 18 are patentable under 35 U.S.C. § 102(b) over Usami; whether claims 19-24 are patentable under 35 U.S.C. § 103(a) over Usami; and whether claims 17-24 are patentable under 35 U.S.C. § 103(a) over Usami in view of Sakamoto.
- IV. Whether claims 25-30 are patentable under 35 U.S.C. § 103(a) over Usami and whether claims 25-30 are patentable under 35 U.S.C. § 103(a) over Usami in view of Sakamoto.
- V. Whether claims 34-38 are patentable under 35 U.S.C. § 103(a) over Usami and whether claims 34-38 are patentable under 35 U.S.C. § 103(a) over Usami in view of Sakamoto.

ARGUMENT

I. The Applicable Law

With regard to a 35 U.S.C. § 102(b) anticipation rejection: "A person shall be entitled to a patent unless- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States." 35 U.S.C. § 102(b).

A rejection based on 35 U.S.C. § 102(b) can be overcome by: persuasively arguing that the claims are patentably distinguishable from the prior art; or, amending the claims to patentably distinguish over the prior art. M.P.E.P. § 706.02(b).

The rejections set forth in the Final Office Action have as their basis 35 U.S.C. §103(a), stating:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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Patent Examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case. MPEP §2141. The Examiner bears the burden under 35 U.S.C. §103 in establishing a *prima facie* case of obviousness. *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

The four factual inquiries for determining obviousness are as follows: (a) determining the scope and contents of the prior art; (b) ascertaining the differences between the prior art and the claims in issue; (c) resolving the level of ordinary skill in the pertinent art; and (d) evaluating evidence of secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966).

When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (a) the claimed invention must be considered as a whole; (b) the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (c) the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (d) reasonable expectation of success is the standard with which obviousness is determined. *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

“Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. ___, slip opinion at page 14 (2007); *In re Khan*, 78 USPQ2d 1329 (Fed. Cir. 2006). In this regard, identification of a teaching, suggestion, or motivation for modifying a reference or combination of the teachings of multiple references provides helpful insight. *KSR*, 550 U.S. at ___, slip opinion at page 15.

II. Rejection of claims 1-3 and 31 under 35 U.S.C. § 102(b) as being unpatentable over Usami, U.S. Patent No. 6,205,516 (“Usami”); rejection of claims 4-7, 9-16, 32, and 33 under 35 U.S.C. § 103(a) as being unpatentable over Usami; and rejection of claims 1-7, 9-16, 32, and 33 under 35 U.S.C. § 103(a) as being unpatentable over Usami in view of Sakamoto et al., “A Digitally Programmable Delay Chip with Picosecond Resolution” (“Sakamoto”).

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Independent claims 1 and 31 are patentably distinct from Usami.

Appellant submits that Usami fails to teach or suggest the limitations recited by independent claim 1 including **a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits:

SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3. Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent. (Final Office Action mailed December 12, 2007, page 3).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 1. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir.

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2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 1, the limitations of claim 1 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Further, Usami does not disclose that CAS latencies are varied by changing the number of pipeline stages in a cache as suggested by the Examiner. Usami does not disclose any cache including pipeline stages. In contrast, Usami discloses that CAS latency is designated as the number of clock cycles required until I/O data is actually started being outputted after column address strobe signal CAS is inputted. (Col. 9, lines 28-31).

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit or a circuit configured to select between receiving the data from the memory array to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal as recited in independent claim 1. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency select signal. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive a CAS latency select signal for selecting a pipeline stage. The CAS latency select signal is only provided to column address counter 36.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 1.

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The Examiner submits that “even though a counter is being used the data to be sent to the memory is being stalled in a buffer. In order to achieve a CL-1 then this buffer must be bypassed altogether. Therefore, a bypass circuit, in some form, must inherently be present.” (Final Office Action mailed December 12, 2007, page 4). Usami, however, does not disclose any buffer or bypass circuit that bypasses a buffer in DRAM core 37. In contrast, Usami discloses that column address counter 36 performs its column address counting-and-outputting operation at timings so that the DRAM core bank 37 will perform its I/O data processing operation in a burst type and with a CAS latency, the burst type and the CAS latency being designated also by the mode register 35. (Col. 9, lines 21-26). Therefore, column address counter 36 controls the timing such that DRAM core 37 outputs data having the desired CAS latency to I/O data buffer/register 33. Usami does not disclose that the data from DRAM core 37 is stalled in a buffer to provide the desired CAS latency as suggested by the Examiner.

In view of the above, Appellant respectfully requests reversal of the rejection of independent claim 1 under 35 U.S.C. § 102(b).

Usami and Sakamoto fail to render independent claims 1 and 31 *prima facie* obvious.

For similar reasons as discussed above with reference to claim 1 and for additional reasons discussed below, Appellant submits that Usami and Sakamoto, either alone, or in combination, fail to teach or suggest the limitations recited by independent claim 1.

The Examiner states: “[f]or the purposes of the following rejection Usami fails to disclose a bypass circuit.” (Final Office Action mailed December 12, page 7). The Examiner also states:

Figure 1 shows delay circuitry that receives an input and will then delay the data by use of a chain of multiple buffers. As previously stated, if CL-3 then it will need to be delayed three pipeline stages. This will happen by use of the delay circuit. The input will go into the 32 to 1 multiplexer and through the delay chain of buffers as necessary until the desired delay is achieved. However, when CL-1 is selected there can be no delay. The input will go into the 32 to 1 multiplexer and will immediately be outputted. Therefore at the very least the delay chain of buffers will be bypassed. Therefore the combination of Usami and Sakamoto discloses a bypass circuit. (Final Office Action mailed December 12, 2007, page 9).

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In the Response to Arguments section, the Examiner states that Sakamoto is relied upon to teach a delay circuit. (Final Office Action mailed December 12, 2007, page 14).

The Examiner admitted for purposes of the rejection that Usami fails to disclose a bypass circuit. The Examiner relied on Sakamoto to teach a delay circuit and not a bypass circuit. Therefore, the Examiner has admitted that neither Usami nor Sakamoto disclose a *bypass circuit*. As shown in Figure 1 of Sakamoto, the input signals IN and INB pass through a first delay buffer before they are input to input (0) of the 32 to 1 multiplexer. Therefore, the output of the 32 to 1 multiplexer must be delayed, as is the purpose of the delay circuit. Sakamoto does not disclose that the input will go into the 32 to 1 multiplexer and will immediately be outputted as suggested by the Examiner. The delay circuit of Sakamoto does not include a bypass option. The delay buffers cannot be bypassed in the delay circuit of Sakamoto as suggested by the Examiner. The Examiner states that when CL-1 is selected there can be no delay, but as illustrated in Figure 3 of Sakamoto, the minimum delay of the delay circuit is about 1900 ps.

Further, the Examiner submits it would have been obvious to utilize the delay circuitry of Sakamoto as the counter delay in Usami. (Final Office Action mailed December 12, 2007, page 9). In the Response to Arguments section, the Examiner states "Usami discloses a memory with a programmable CAS latency. Usami uses a counter to introduce the delay, as needed, into the circuit to add pseudo-pipeline stages. Therefore, Usami does disclose a delay counter." (Final Office Action mailed December 12, 2007, page 14). Usami does not disclose any delay counter. Usami only discloses a column address counter 36 and an I/O data buffer/register 33. The delay circuitry of Sakamoto could not be used for column address counter 36 of Usami. Such a use would render column address counter 36 unsuitable for its intended purpose. One skilled in the art could not combine the delay circuitry of Sakamoto with the device of Usami to provide a *bypass circuit* as recited by independent claim 1.

In view of the above, Appellant respectfully requests reversal of the rejection of independent claim 1 under 35 U.S.C. § 103(a). Dependent claims 2-7 and 9-16 further define patentably distinct independent claim 1. Accordingly, Appellant believes that these dependent claims are also allowable over the cited references. Appellant respectfully

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requests reversal of the rejection of claims 2-3 under 35 U.S.C. § 102(b) and the rejections of claims 2-7 and 9-16 under 35 U.S.C. § 103(a).

For the same reasons as discussed above with reference to claim 1, Appellant submits that Usami and Sakamoto, either alone, or in combination, fail to teach or suggest the limitations recited by independent claim 31 including **means for receiving the data read from the array of memory cells to bypass the means for storing data; means for retrieving the data from the means for storing the data if column address strobe latency is greater than one; means for retrieving the data from the means for receiving the data if the column address strobe latency is one.**

In view of the above, Appellant respectfully requests reversal of the rejection of independent claim 31 under 35 U.S.C. § 102(b) and the rejection of independent claim 31 under 35 U.S.C. § 103(a). Dependent claims 32 and 33 further define patentably distinct independent claim 31. Accordingly, Appellant believes that these dependent claims are also allowable over the cited references. Appellant respectfully requests reversal of the rejections of claims 32 and 33 under 35 U.S.C. § 103(a).

III. Rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Usami and rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Usami in view of Sakamoto.

Usami fails to render claim 8 *prima facie* obvious.

Appellant submits that Usami fails to teach or suggest the invention recited by dependent claim 8 including **a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal, wherein the circuit comprises a first circuit configured to receive first rise and fall signals to serialize the data from the memory, wherein the circuit comprises a second circuit configured to receive second rise and fall signals to serialize the data from the bypass circuit, and wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and**

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serialized data from the second circuit based on the column address strobe latency select signal.

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits:

SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3. Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent. (Final Office Action mailed December 12, 2007, page 3).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 8. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 8, the limitations of claim 8 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

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Further, Usami does not disclose that CAS latencies are varied by changing the number of pipeline stages in a cache as suggested by the Examiner. Usami does not disclose any cache including pipeline stages. In contrast, Usami discloses that CAS latency is designated as the number of clock cycles required until I/O data is actually started being outputted after column address strobe signal CAS is inputted. (Col. 9, lines 28-31).

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit or a circuit configured to select between receiving the data from the memory array to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal as recited in claim 8. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency select signal. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive a CAS latency select signal for selecting a pipeline stage. The CAS latency select signal is only provided to column address counter 36.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 8.

The Examiner submits that "even though a counter is being used the data to be sent to the memory is being stalled in a buffer. In order to achieve a CL-1 then this buffer must be bypassed altogether. Therefore, a bypass circuit, in some form, must inherently be present." (Final Office Action mailed December 12, 2007, page 4). Usami, however, does not disclose any buffer or bypass circuit that bypasses the buffer in DRAM core 37. In contrast, Usami

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discloses that column address counter 36 performs its column address counting-and-outputting operation at timings so that the DRAM core bank 37 will perform its I/O data processing operation in a burst type and with a CAS latency, the burst type and the CAS latency being designated also by the mode register 35. (Col. 9, lines 21-26). Therefore, column address counter 36 controls the timing such that DRAM core 37 outputs data having the desired CAS latency to I/O data buffer/register 33. Usami does not disclose that the data from DRAM core 37 is stalled in a buffer to provide the desired CAS latency as suggested by the Examiner.

Further, there is no teaching or suggestion in Usami of a first circuit to serialize the data from the memory and a second circuit to serialize the data from the bypass circuit. In addition, there is no teaching or suggestion in Usami of a multiplexer, let alone a multiplexer configured to select between data from the first circuit and data from the second circuit based on the CAS latency select signal. In contrast, Usami discloses a single circuit, I/O data buffer register 33, for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. (Col. 9, lines 63-66). Regarding these limitations, the Examiner states:

A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed. (Final Office Action mailed December 12, 2007, page 5).

Usami, however, fails to teach or suggest these claim limitations. In Addition, Appellant submits that a first circuit to serialize the data from the memory, a second circuit to serialize the data from the bypass circuit, and a multiplexer configured to select between data from the first circuit and data from the second circuit are not inherent in Usami. As the Federal Circuit has stated, “[i]nherent anticipation requires that the missing descriptive material is ‘necessarily present,’ not merely probably or possibly present, in the prior art.” *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re*

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Robertson, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since serializing data in Usami could be performed without utilizing each of a first circuit, a second circuit, and a multiplexer as recited in claim 8, the limitations of claim 8 are not inherent in Usami as submitted by the Examiner.

In the Response to Arguments section, the Examiner states that “Usami teaches that CAS latency is determined based on the CAS latency bits of Figure 4. The mode register is this sense functions as the multiplexer by taking the control signal (the latency bits) and interpreting it to determine the bypassing of the stall buffer or not.” (Final Office Action mailed December 12, 2007, pages 13-14). Mode register 35 is not a multiplexer and cannot function as a multiplexer. Mode register 35 also does not determine whether a stall buffer is bypassed. Usami does not disclose a stall buffer. In contrast, Usami discloses that mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined “mode register set” command that is received from the command decoder 31. The mode register 35 is also for storing the executed operation mode information therein. According to the operation mode information designated by the address data A0-A11, the mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling the count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, mode register 35 is not configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal.

Usami and Sakamoto fail to render claim 8 *prima facie* obvious.

For similar reasons as discussed above with reference to claim 8 and for additional reasons discussed below, Appellant submits that Usami and Sakamoto, either alone, or in combination, fail to teach or suggest the limitations recited by claim 8.

The Examiner states: “[f]or the purposes of the following rejection Usami fails to disclose a bypass circuit.” (Final Office Action mailed December 12, page 7). The Examiner also states:

Figure 1 shows delay circuitry that receives an input and will then delay the data by use of a chain of multiple buffers. As previously stated, if CL-3 then it

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will need to be delayed three pipeline stages. This will happen by use of the delay circuit. The input will go into the 32 to 1 multiplexer and through the delay chain of buffers as necessary until the desired delay is achieved. However, when CL-1 is selected there can be no delay. The input will go into the 32 to 1 multiplexer and will immediately be outputted. Therefore at the very least the delay chain of buffers will be bypassed. Therefore the combination of Usami and Sakamoto discloses a bypass circuit. (Final Office Action mailed December 12, 2007, page 9).

In the Response to Arguments section, the Examiner states that Sakamoto is relied upon to teach a delay circuit. (Final Office Action mailed December 12, 2007, page 14).

The Examiner admitted for purposes of the rejection that Usami fails to disclose a bypass circuit. The Examiner relied on Sakamoto to teach a delay circuit and not a bypass circuit. Therefore, the Examiner has admitted that neither Usami nor Sakamoto disclose a *bypass circuit*. As shown in Figure 1 of Sakamoto, the input signals IN and INB pass through a first delay buffer before they are input to input (0) of the 32 to 1 multiplexer. Therefore, the output of the 32 to 1 multiplexer must be delayed, as is the purpose of the delay circuit. Sakamoto does not disclose that the input will go into the 32 to 1 multiplexer and will immediately be outputted as suggested by the Examiner. The delay circuit of Sakamoto does not include a bypass option. The delay buffers cannot be bypassed in the delay circuit of Sakamoto as suggested by the Examiner. The Examiner states that when CL-1 is selected there can be no delay, but as illustrated in Figure 3 of Sakamoto, the minimum delay of the delay circuit is about 1900 ps.

Further, the Examiner submits it would have been obvious to utilize the delay circuitry of Sakamoto as the counter delay in Usami. (Final Office Action mailed December 12, 2007, page 9). In the Response to Arguments section, the Examiner states: "Usami discloses a memory with a programmable CAS latency. Usami uses a counter to introduce the delay, as needed, into the circuit to add pseudo-pipeline stages. Therefore, Usami does disclose a delay counter." (Final Office Action mailed December 12, 2007, page 14). Usami does not disclose a delay counter. Usami only discloses a column address counter 36 and an I/O data buffer/register 33. The delay circuitry of Sakamoto could not be used for column address counter 36 of Usami. Such a use would render column address counter 36 unsuitable for its intended purpose. One skilled in the art could not combine the delay circuitry of Sakamoto with the device of Usami to provide a *bypass circuit* as recited by claim 8.

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In view of the above, Appellant respectfully requests reversal of the rejections of claim 8 under 35 U.S.C. § 103(a).

IV. Rejection of claims 17 and 18 under 35 U.S.C. § 102(b) as being unpatentable over Usami; rejection of claims 19-24 under 35 U.S.C. § 103(a) as being unpatentable over Usami; and rejection of claims 17-24 under 35 U.S.C. § 103(a) as being unpatentable over Usami in view of Sakamoto.

Independent claim 17 is patentably distinct from Usami.

Appellant submits that Usami fails to teach or suggest the invention recited by independent claim 17 including **a bypass circuit that bypasses the first in/first out memory; and a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits:

SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3. Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select

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between receiving data are inherent. (Final Office Action mailed December 12, 2007, page 3).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 17. As the Federal Circuit has stated, “[i]nherent anticipation requires that the missing descriptive material is ‘necessarily present,’ not merely probably or possibly present, in the prior art.” *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 8, the limitations of claim 8 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Further, Usami does not disclose that CAS latencies are varied by changing the number of pipeline stages in a cache as suggested by the Examiner. Usami does not disclose any cache including pipeline stages. In contrast, Usami discloses that CAS latency is designated as the number of clock cycles required until I/O data is actually started being outputted after column address strobe signal CAS is inputted. (Col. 9, lines 28-31).

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit or a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one as recited in independent claim 17. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive first and second signals from a control circuit for selecting a pipeline stage.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined “mode

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register set” command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 17.

The Examiner submits: “even though a counter is being used the data to be sent to the memory is being stalled in a buffer. In order to achieve a CL-1 then this buffer must be bypassed altogether. Therefore, a bypass circuit, in some form, must inherently be present.” (Final Office Action mailed December 12, 2007, page 4). Usami, however, does not disclose any buffer or bypass circuit that bypasses the buffer in DRAM core 37. In contrast, Usami discloses that column address counter 36 performs its column address counting-and-outputting operation at timings so that the DRAM core bank 37 will perform its I/O data processing operation in a burst type and with a CAS latency, the burst type and the CAS latency being designated also by the mode register 35. (Col. 9, lines 21-26). Therefore, column address counter 36 controls the timing such that DRAM core 37 outputs data having the desired CAS latency to I/O data buffer/register 33. Usami does not disclose that the data from DRAM core 37 is stalled in a buffer to provide the desired CAS latency as suggested by the Examiner.

In view of the above, Appellant respectfully requests reversal of the rejection of independent claim 17 under 35 U.S.C. § 102(b).

Usami and Sakamoto fail to render independent claim 17 *prima facie* obvious.

For similar reasons as discussed above with reference to independent claim 17 and for additional reasons discussed below, Appellant submits that Usami and Sakamoto, either alone, or in combination, fail to teach or suggest the limitations recited by independent claim 17.

The Examiner states: “[f]or the purposes of the following rejection Usami fails to disclose a bypass circuit.” (Final Office Action mailed December 12, page 7). The Examiner also states:

Figure 1 shows delay circuitry that receives an input and will then delay the data by use of a chain of multiple buffers. As previously stated, if CL-3 then it

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will need to be delayed three pipeline stages. This will happen by use of the delay circuit. The input will go into the 32 to 1 multiplexer and through the delay chain of buffers as necessary until the desired delay is achieved. However, when CL-1 is selected there can be no delay. The input will go into the 32 to 1 multiplexer and will immediately be outputted. Therefore at the very least the delay chain of buffers will be bypassed. Therefore the combination of Usami and Sakamoto discloses a bypass circuit. (Final Office Action mailed December 12, 2007, page 9).

In the Response to Arguments section, the Examiner states that Sakamoto is relied upon to teach a delay circuit. (Final Office Action mailed December 12, 2007, page 14).

The Examiner admitted for purposes of the rejection that Usami fails to disclose a bypass circuit. The Examiner relied on Sakamoto to teach a delay circuit and not a bypass circuit. Therefore, the Examiner has admitted that neither Usami nor Sakamoto disclose a *bypass circuit*. As shown in Figure 1 of Sakamoto, the input signals IN and INB pass through a first delay buffer before they are input to input (0) of the 32 to 1 multiplexer. Therefore, the output of the 32 to 1 multiplexer must be delayed, as is the purpose of the delay circuit. Sakamoto does not disclose that the input will go into the 32 to 1 multiplexer and will immediately be outputted as suggested by the Examiner. The delay circuit of Sakamoto does not include a bypass option. The delay buffers cannot be bypassed in the delay circuit of Sakamoto as suggested by the Examiner. The Examiner states that when CL-1 is selected there can be no delay, but as illustrated in Figure 3 of Sakamoto, the minimum delay of the delay circuit is about 1900 ps.

Further, the Examiner submits it would have been obvious to utilize the delay circuitry of Sakamoto as the counter delay in Usami. (Final Office Action mailed December 12, 2007, page 9). In the Response to Arguments section, the Examiner states "Usami discloses a memory with a programmable CAS latency. Usami uses a counter to introduce the delay, as needed, into the circuit to add pseudo-pipeline stages. Therefore, Usami does disclose a delay counter." (Final Office Action mailed December 12, 2007, page 14). Usami does not disclose any delay counter. Usami only discloses a column address counter 36 and an I/O data buffer/register 33. The delay circuitry of Sakamoto could not be used for column address counter 36 of Usami. Such a use would render column address counter 36 unsuitable for its intended purpose. One skilled in the art could not combine the delay circuitry of

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Sakamoto with the device of Usami to provide a *bypass circuit* as recited by independent claim 17.

In view of the above, Appellant respectfully requests reversal of the rejection of independent claim 17 under 35 U.S.C. § 103(a). Dependent claims 18-24 further define patentably distinct independent claim 17. Accordingly, Appellant believes that these dependent claims are also allowable over the cited references. Appellant respectfully requests reversal of the rejection of claim 18 under 35 U.S.C. § 102(b) and the rejections of claims 18-24 under 35 U.S.C. § 103(a).

V. Rejection of claims 25-30 under 35 U.S.C. § 103(a) as being unpatentable over Usami and rejection of claims 25-30 under 35 U.S.C. § 103(a) as being unpatentable over Usami in view of Sakamoto.

Usami fails to render independent claim 25 *prima facie* obvious.

Appellant submits that Usami fails to teach or suggest the invention recited by independent claim 25 including **a bypass circuit configured to bypass the memory circuit; a first rise/fall circuit configured to receive data from the memory circuit to provide a first output signal; a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal; and a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits:

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SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3. Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent. (Final Office Action mailed December 12, 2007, page 3).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 25. As the Federal Circuit has stated, “[i]nherent anticipation requires that the missing descriptive material is ‘necessarily present,’ not merely probably or possibly present, in the prior art.” *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since varying the CAS latency in Usami could be performed without utilizing a bypass circuit as recited in claim 25, the limitations of claim 25 are not inherent in Usami as submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Further, Usami does not disclose that CAS latencies are varied by changing the number of pipeline stages in the cache as suggested by the Examiner. Usami does not disclose any cache including pipeline stages. In contrast, Usami discloses that CAS latency is designated as the number of clock cycles required until I/O data is actually started being outputted after column address strobe signal CAS is inputted. (Col. 9, lines 28-31).

Figures 2 and 4 and the associated text of Usami do not disclose a bypass circuit. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency select signal. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages. Even if I/O data buffer/register 33 did include pipeline stages, I/O data buffer/register 33 does not receive a CAS latency select

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signal for selecting a pipeline stage. The CAS latency select signal is only provided to column address counter 36.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 25.

The Examiner submits: "even though a counter is being used the data to be sent to the memory is being stalled in a buffer. In order to achieve a CL-1 then this buffer must be bypassed altogether. Therefore, a bypass circuit, in some form, must inherently be present." (Final Office Action mailed December 12, 2007, page 4). Usami, however, does not disclose any buffer or bypass circuit that bypasses the buffer in DRAM core 37. In contrast, Usami discloses that column address counter 36 performs its column address counting-and-outputting operation at timings so that the DRAM core bank 37 will perform its I/O data processing operation in a burst type and with a CAS latency, the burst type and the CAS latency being designated also by the mode register 35. (Col. 9, lines 21-26). Therefore, column address counter 36 controls the timing such that DRAM core 37 outputs data having the desired CAS latency to I/O data buffer/register 33. Usami does not disclose that the data from DRAM core 37 is stalled in a buffer to provide the desired CAS latency as suggested by the Examiner.

Further, there is no teaching or suggestion in Usami of a first rise/fall circuit configured to receive data from the bypass circuit to provide a first output signal and a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal. In addition, there is no teaching or suggestion in Usami of a multiplexer, let alone a multiplexer configured to select between the first output signal and the second output signal based on the CAS latency select signal. In contrast, Usami discloses a single circuit, I/O data buffer register 33, for temporarily storing data to be written to the DRAM core 37 or for

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temporarily storing data read from the DRAM core 37. (Col. 9, lines 63-66). Regarding these limitations, the Examiner states:

A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed. (Final Office Action mailed December 12, 2007, page 5).

Usami, however, fails to teach or suggest these claim limitations. In Addition, Appellant submits that a first rise/fall circuit configured to receive data from the memory to provide a first output signal, a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal, and a multiplexer configured to select between the first output signal and the second output signal are not inherent in Usami. As the Federal Circuit has stated, “[i]nherent anticipation requires that the missing descriptive material is ‘necessarily present,’ not merely probably or possibly present, in the prior art.” *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since serializing data in Usami could be performed without utilizing each of a first rise/fall circuit, a second rise/fall circuit, and a multiplexer as recited in claim 25, the limitations of claim 25 are not inherent in Usami as submitted by the Examiner.

In the Response to Arguments section, the Examiner states: “Usami teaches that CAS latency is determined based on the CAS latency bits of Figure 4. The mode register is this sense functions as the multiplexer by taking the control signal (the latency bits) and interpreting it to determine the bypassing of the stall buffer or not.” (Final Office Action mailed December 12, 2007, pages 13-14). Mode register 35 is not a multiplexer and cannot function as a multiplexer. Mode register 35 also does not determine whether a stall buffer is bypassed. Usami does not disclose a stall buffer. In contrast, Usami discloses that mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives

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the address data A0-A11 in correspondence with a predetermined “mode register set” command that is received from the command decoder 31. The mode register 35 is also for storing the executed operation mode information therein. According to the operation mode information designated by the address data A0-A11, the mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling the count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, mode register 35 is not configured to select between the first output signal and the second output signal based on the column address strobe latency select signal.

Usami and Sakamoto fail to render independent claim 25 *prima facie* obvious.

For similar reasons as discussed above with reference to independent claim 25 and for additional reasons discussed below, Appellant submits that Usami and Sakamoto, either alone, or in combination, fail to teach or suggest the limitations recited by independent claim 25.

The Examiner states: “[f]or the purposes of the following rejection Usami fails to disclose a bypass circuit.” (Final Office Action mailed December 12, page 7). The Examiner also states:

Figure 1 shows delay circuitry that receives an input and will then delay the data by use of a chain of multiple buffers. As previously stated, if CL-3 then it will need to be delayed three pipeline stages. This will happen by use of the delay circuit. The input will go into the 32 to 1 multiplexer and through the delay chain of buffers as necessary until the desired delay is achieved. However, when CL-1 is selected there can be no delay. The input will go into the 32 to 1 multiplexer and will immediately be outputted. Therefore at the very least the delay chain of buffers will be bypassed. Therefore the combination of Usami and Sakamoto discloses a bypass circuit. (Final Office Action mailed December 12, 2007, page 9).

In the Response to Arguments the Examiner states that Sakamoto is relied upon to teach a delay circuit. (Final Office Action mailed December 12, 2007, page 14).

The Examiner admitted for purposes of the rejection that Usami fails to disclose a bypass circuit. The Examiner relied on Sakamoto to teach a delay circuit and not a bypass circuit. Therefore, the Examiner has admitted that neither Usami nor Sakamoto disclose a *bypass circuit*. As shown in Figure 1 of Sakamoto, the input signals IN and INB pass

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through a first delay buffer before they are input to input (0) of the 32 to 1 multiplexer. Therefore, the output of the 32 to 1 multiplexer must be delayed, as is the purpose of the delay circuit. Sakamoto does not disclose that the input will go into the 32 to 1 multiplexer and will immediately be outputted as suggested by the Examiner. The delay circuit of Sakamoto does not include a bypass option. The delay buffers cannot be bypassed in the delay circuit of Sakamoto as suggested by the Examiner. The Examiner states that when CL-1 is selected there can be no delay, but as illustrated in Figure 3 of Sakamoto, the minimum delay of the delay circuit is about 1900 ps.

Further, the Examiner submits it would have been obvious to utilize the delay circuitry of Sakamoto as the counter delay in Usami. (Final Office Action mailed December 12, 2007, page 9). In the Response to Arguments section, the Examiner states "Usami discloses a memory with a programmable CAS latency. Usami uses a counter to introduce the delay, as needed, into the circuit to add pseudo-pipeline stages. Therefore, Usami does disclose a delay counter." (Final Office Action mailed December 12, 2007, page 14). Usami does not disclose any delay counter. Usami only discloses a column address counter 36 and an I/O data buffer/register 33. The delay circuitry of Sakamoto could not be used for column address counter 36 of Usami. Such a use would render column address counter 36 unsuitable for its intended purpose. One skilled in the art could not combine the delay circuitry of Sakamoto with the device of Usami to provide a *bypass circuit* as recited by independent claim 25.

In view of the above, Appellant respectfully requests reversal of the rejections of claim 25 under 35 U.S.C. § 103(a). Dependent claims 26-30 further define patentably distinct independent claim 25. Accordingly, Appellant believes that these dependent claims are also allowable over the cited references. Appellant respectfully requests reversal of the rejections of claims 26-30 under 35 U.S.C. § 103(a).

VI. Rejection of claims 34-38 under 35 U.S.C. § 103(a) as being unpatentable over Usami and rejection of claims 34-38 under 35 U.S.C. § 103(a) as being unpatentable over Usami in view of Sakamoto.

Usami fails to render independent claim 34 *prima facie* obvious.

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Appellant submits that Usami fails to teach or suggest the invention recited by independent claim 34 including **receiving data read from the array of memory cells in a bypass circuit during the clock cycle; and retrieving the data from the bypass circuit during the clock cycle.**

Usami discloses that each SDRAM includes a DRAM core 37. The DRAM core 37 is constructed from a plurality of banks. The SDRAM further includes a clock buffer 30, a command decoder 31, an address buffer/register and bank select 32, a pair of control signal latches 34, a mode register 35, a pair of column address counters 36, and an I/O data buffer/register 33. (Col. 7, line 64 - col. 8, line 3). The I/O data buffer/register 33 serves as a buffer circuit or register circuit for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. The I/O data buffer/register 33 is connected to the corresponding data bus "I/O data DQ0-DQ3" that is connected to the CPU 1. (Col. 9, lines 62 - col. 10, line 1).

The Examiner submits:

SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS latency) will vary accordingly as described in Claims 2 and 3. Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent. (Final Office Action mailed December 12, 2007, page 3).

Appellant submits that it is not inherent in Usami that a bypass circuit is used as recited in claim 34. As the Federal Circuit has stated, "[i]nherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since providing a CAS latency of one in Usami could be performed without utilizing a bypass circuit as recited in claim 34, the limitations of claim 34 are not inherent in Usami as

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submitted by the Examiner. In addition, there is not a single reference to a cache memory including pipeline stages in Usami.

Further, Usami does not disclose that CAS latencies are varied by changing the number of pipeline stages in the cache as suggested by the Examiner. Usami does not disclose any cache including pipeline stages. In contrast, Usami discloses that CAS latency is designated as the number of clock cycles required until I/O data is actually started being outputted after column address strobe signal CAS is inputted. (Col. 9, lines 28-31).

Figures 2 and 4 and the associated text of Usami do not disclose receiving data read from the array of memory cells in a bypass circuit during the clock cycle or receiving the data from the bypass circuit during the clock cycle as recited in independent claim 34. In contrast, Usami merely discloses an I/O data buffer/register 33 for receiving data from the DRAM core 37 or writing data to the DRAM core 37. Nowhere in the text or figures does Usami disclose a bypass circuit for routing the data around I/O data buffer/register 33 based on a column address strobe latency of one. There is also no teaching or suggestion that I/O data buffer/register 33 includes pipeline stages.

The mode register 35 is for extracting operation mode information, such as the CAS latency, the burst type, and the burst length, from the address data A0-A11 when the mode register 35 receives the address data A0-A11 in correspondence with a predetermined "mode register set" command that is received from the command decoder 31. Mode register 35 supplies each column address counter 36 with a control signal designating the burst length, the burst type, and the CAS latency, thereby controlling count up timing and count up number of the column address counter 36. (Col. 9, lines 45-62). Therefore, Usami discloses controlling the CAS latency based on controlling the column address counter 36, not by using a bypass circuit as recited in claim 34.

Further, there is no teaching or suggestion in Usami of receiving the data from the bypass circuit during the clock cycle that initiated the read command. In contrast, Usami discloses a single circuit, I/O data buffer register 33, for temporarily storing data to be written to the DRAM core 37 or for temporarily storing data read from the DRAM core 37. (Col. 9, lines 63-66). Regarding these limitations, the Examiner states:

A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner

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takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed. (Final Office Action mailed December 12, 2007, page 5).

Usami, however, fails to teach or suggest these claim limitations. In Addition, Appellant submits that retrieving the data from a bypass circuit during the clock cycle that initiated a read command is not inherent in Usami. As the Federal Circuit has stated, “[i]nherent anticipation requires that the missing descriptive material is ‘necessarily present,’ not merely probably or possibly present, in the prior art.” *Trintec Indus., v. Top-U.S.A. Corp.*, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Since a CAS latency of one in Usami could be provided without retrieving the data from a bypass circuit during the clock cycle as recited in claim 34, the limitations of claim 34 are not inherent in Usami as submitted by the Examiner.

Usami and Sakamoto fail to render independent claim 34 *prima facie* obvious.

For similar reasons as discussed above with reference to independent claim 34 and for additional reasons discussed below, Appellant submits that Usami and Sakamoto, either alone, or in combination, fail to teach or suggest the limitations recited by independent claim 34.

The Examiner states: “[f]or the purposes of the following rejection Usami fails to disclose a bypass circuit.” (Final Office Action mailed December 12, page 7). The Examiner also states:

Figure 1 shows delay circuitry that receives an input and will then delay the data by use of a chain of multiple buffers. As previously stated, if CL-3 then it will need to be delayed three pipeline stages. This will happen by use of the delay circuit. The input will go into the 32 to 1 multiplexer and through the delay chain of buffers as necessary until the desired delay is achieved. However, when CL-1 is selected there can be no delay. The input will go into the 32 to 1 multiplexer and will immediately be outputted. Therefore at the very least the delay chain of buffers will be bypassed. Therefore the combination of Usami and Sakamoto discloses a bypass circuit. (Final Office Action mailed December 12, 2007, page 9).

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In the Response to Arguments the Examiner states that Sakamoto is relied upon to teach a delay circuit. (Final Office Action mailed December 12, 2007, page 14).

The Examiner admitted for purposes of the rejection that Usami fails to disclose a bypass circuit. The Examiner relied on Sakamoto to teach a delay circuit and not a bypass circuit. Therefore, the Examiner has admitted that neither Usami nor Sakamoto disclose a *bypass circuit*. As shown in Figure 1 of Sakamoto, the input signals IN and INB pass through a first delay buffer before they are input to input (0) of the 32 to 1 multiplexer. Therefore, the output of the 32 to 1 multiplexer must be delayed, as is the purpose of the delay circuit. Sakamoto does not disclose that the input will go into the 32 to 1 multiplexer and will immediately be outputted as suggested by the Examiner. The delay circuit of Sakamoto does not include a bypass option. The delay buffers cannot be bypassed in the delay circuit of Sakamoto as suggested by the Examiner. The Examiner states that when CL-1 is selected there can be no delay, but as illustrated in Figure 3 of Sakamoto, the minimum delay of the delay circuit is about 1900 ps.

Further, the Examiner submits it would have been obvious to utilize the delay circuitry of Sakamoto as the counter delay in Usami. (Final Office Action mailed December 12, 2007, page 9). In the Response to Arguments section, the Examiner states: "Usami discloses a memory with a programmable CAS latency. Usami uses a counter to introduce the delay, as needed, into the circuit to add pseudo-pipeline stages. Therefore, Usami does disclose a delay counter." (Final Office Action mailed December 12, 2007, page 14). Usami does not disclose any delay counter. Usami only discloses a column address counter 36 and an I/O data buffer/register 33. The delay circuitry of Sakamoto could not be used for column address counter 36 of Usami. Such a use would render column address counter 36 unsuitable for its intended purpose. One skilled in the art could not combine the delay circuitry of Sakamoto with the device of Usami to provide a *bypass circuit* as recited by independent claim 34.

In view of the above, Appellant respectfully requests reversal of the rejections of claim 34 under 35 U.S.C. § 103(a). Dependent claims 35-38 further define patentably distinct independent claim 34. Accordingly, Appellant believes that these dependent claims are also allowable over the cited references. Appellant respectfully requests reversal of the rejections of claims 35-38 under 35 U.S.C. § 103(a).

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CONCLUSION

For the above reasons, Appellant respectfully submits that the cited references neither anticipate nor render obvious claims of the pending Application. The pending claims distinguish over the cited references, and therefore Appellant respectfully submits that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-38 be allowed.

Any inquiry regarding this Appeal Brief should be directed to Mark A. Peterson at Telephone No. (612) 573-0120, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Dicke, Billig & Czaja
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

Respectfully submitted,

Torsten Partsch,

By his attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-0120
Facsimile: (612) 573-2005

Dated: _____

MAP:kmh

4/11/2008

Mark Peterson

Mark A. Peterson

Reg. No. 50,485

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CLAIMS APPENDIX

1. (Previously Presented) A random access memory, comprising:
 - an array of memory cells;
 - a memory configured to receive data from the array of memory cells;
 - a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and
 - a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal.
2. (Previously Presented) The random access memory of claim 1, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency select signal indicates a column address strobe latency value of one.
3. (Previously Presented) The random access memory of claim 1, wherein the circuit is configured to receive the data from the memory and provide the first output signals if the column address strobe latency select signal indicates a column address strobe latency value of greater than one.
4. (Original) The random access memory of claim 1, wherein the circuit comprises a first circuit configured to receive first rise and fall signals to serialize the data from the memory.
5. (Original) The random access memory of claim 4, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle.
6. (Original) The random access memory of claim 4, wherein the circuit comprises a second circuit configured to receive second rise and fall signals to serialize the data from the bypass circuit.

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7. (Original) The random access memory of claim 6, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle and the second rise and fall signals during the first clock cycle.
8. (Previously Presented) The random access memory of claim 6, wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal.
9. (Original) The random access memory of claim 1, wherein the circuit comprises a rise and fall circuit configured to receive first rise and fall signals to serialize the data from the memory and to receive second rise and fall signals to serialize the data from the bypass circuit.
10. (Previously Presented) The random access memory of claim 9, wherein the circuit is configured to select between providing the first rise and fall signals and providing the second rise and fall signals based on the column address strobe latency select signal.
11. (Original) The random access memory of claim 10, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle and the second rise and fall signals during the first clock cycle.
12. (Previously Presented) The random access memory of claim 1, wherein the bypass circuit is configured to tri-state an output if the column address strobe latency select signal indicates a column address strobe latency value of greater than one.
13. (Original) The random access memory of claim 1, wherein the memory comprises a first in/first out memory.

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14. (Original) The random access memory of claim 1, wherein the random access memory is a low power synchronous dynamic random access memory.
15. (Original) The random access memory of claim 1, wherein the random access memory is a double data rate-I synchronous dynamic random access memory.
16. (Original) The random access memory of claim 1, wherein the random access memory is a double data rate-II synchronous dynamic random access memory.
17. (Original) A random access memory, comprising:
 - a first in/first out memory;
 - a bypass circuit that bypasses the first in/first out memory; and
 - a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one.
18. (Previously Presented) The random access memory of claim 17, wherein the control circuit comprises a clock signal multiplexer configured to select between providing the first signals and the second signals based on a column address strobe latency select signal.
19. (Original) The random access memory of claim 17, comprising a rise/fall circuit configured to receive the first signals and the second signals to provide one data bit at a time.
20. (Original) The random access memory of claim 19, wherein the control circuit is configured to provide the first signals comprising a first rise signal and a first fall signal that is the inverse of the first rise signal and the second signals comprising a second rise signal and a second fall signal that is the inverse of the second rise signal.

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21. (Original) The random access memory of claim 20, wherein the rise/fall circuit is configured to provide a first data bit as output on a rising edge of the first rise signal and a second data bit as output on a rising edge of the first fall signal.
22. (Original) The random access memory of claim 19, comprising a data delay circuit electrically coupled to the rise/fall circuit and configured to adjust output timing of the data.
23. (Original) The random access memory of claim 22, comprising an off chip driver configured to pass data from the data delay circuit to a data pad.
24. (Original) The random access memory of claim 17, wherein the bypass comprises a tri-state output that is set to a high impedance state for the column address strobe latency of greater than one.
25. (Previously Presented) A random access memory, comprising:
a memory circuit;
a bypass circuit configured to bypass the memory circuit;
a first rise/fall circuit configured to receive data from the memory circuit to provide a first output signal;
a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal; and
a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal.
26. (Previously Presented) The random access memory of claim 25, wherein the multiplexer selects the first output signal if the column address strobe latency signal indicates the column address strobe latency is greater than one and the second output signal if the column address strobe latency select signal indicates the column address strobe latency is one.

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27. (Original) The random access memory of claim 25, comprising a controller configured to provide a first signal and a second signal to the first rise/fall circuit and a third signal and a fourth signal to the second rise/fall circuit.

28. (Original) The random access memory of claim 27, wherein the controller is configured to create the first signal and the second signal from a clock signal and the third signal and the fourth signal from the inverted clock signal.

29. (Original) The random access memory of claim 28, wherein the first rise/fall circuit outputs a first data bit on a rising edge of the first signal and a second data bit on a rising edge of the second signal.

30. (Original) The random access memory of claim 28, wherein the second rise/fall circuit outputs a first data bit on a rising edge of the third signal and a second data bit on a rising edge of the fourth signal.

31. (Original) A random access memory comprising:
means for storing data read from an array of memory cells;
means for receiving the data read from the array of memory cells to bypass the means for storing data;
means for retrieving the data from the means for storing the data if column address strobe latency is greater than one;
means for retrieving the data from the means for receiving the data if the column address strobe latency is one.

32. (Original) The random access memory of claim 31, wherein the means for storing data comprises a first in/first out memory.

33. (Original) The random access memory of claim 31, comprising means for serializing the data retrieved from the means for storing and the means for receiving to provide serial data bit output signals.

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34. (Original) A method for reading data from a random access memory in a column address strobe latency of one, comprising:
- initiating a read command on a first edge of a clock cycle;
 - receiving data read from the array of memory cells in a bypass circuit during the clock cycle; and
 - retrieving the data from the bypass circuit during the clock cycle.
35. (Original) The method of claim 34, comprising bypassing first in/first out memory cells used to provide data if the column address strobe latency is greater than one.
36. (Original) The method of claim 34, comprising:
- generating an inverted clock signal from a data clock signal to retrieve the data from the bypass circuit.
37. (Original) The method of claim 36, comprising:
- generating a first signal and a second signal from the inverted clock signal to retrieve the data from the bypass circuit.
38. (Original) The method of claim 37, comprising outputting a first data bit on a rising edge of the first signal and a second data bit on a rising edge of the second signal.

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EVIDENCE APPENDIX

None.

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RELATED PROCEEDINGS APPENDIX

None.